



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Group Art Unit: 2827

Application No.: 09/486,556

Examiner: I. Patel

Filed: February 29, 2000

Docket No.: 105029

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF,
CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

SUPPLEMENTAL REMARKS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

0602

Further to the May 6, 2003 Amendment, and prior to further action on the merits,
please consider the additional remarks below.

Applicant thanks Examiners Cuneo and Patel for the courtesy extended to Applicant's
representative, Mr. Luo, during the May 8, 2003 personal interview. The substance of the
interview is incorporated in the following remarks.

As discussed during the interview, the limitation "substantially flat" recited in claims
30, 50, 68 and 74 is supported in the specification. For example, the specification discloses
on page 19, lines 19-21, that the electrodes 22 of the semiconductor chip 20 and the
interconnect pattern 10 are electrically connected, as shown in Fig. 4B. In Fig. 4B, the
portion of the interconnect pattern 10 that is in contact with the electrode 22 is not obviously
displaced from the rest of the interconnect pattern 10. Fig. 4B clearly shows that that portion
of the interconnect pattern 10 remains substantially flat.

For at least the above reasons, the limitation "substantially flat" is supported in the specification.

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 30-85 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,



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JAO:GXL/vgp

Date: May 15, 2003

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